

	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	1	6297104.pn.	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2002/03/28 21:43
2	BRS	L2	5	5840602.pn. or 6150243.pn.	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2002/03/28 21:46
3	BRS	L3	2984	(logic adj1 device) and (memory adj1 device)	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2002/03/28 21:47
4	BRS	L4	44	(first adj1 transistor) near10 dielectric adj1 layer	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2002/03/28 21:55
5	BRS	L5	4	3 and 4	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2002/03/28 21:51

	Type	L #	Hits	Search Text	DBs	Time Stamp
7	EPG	L6	49	(first adj1 transistor) near15 (dielectric adj1 layer)	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2002/03/28 21:56
					USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2002/03/28 21:56
	EPG	L8	3163	(transistor) near15 (dielectric adj1 layer)	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2002/03/28 22:36
9	EPG	L9	79	3 and 8	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2002/03/28 21:57
10	EPG	L10	69	9 and thickness	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2002/03/28 21:57

	Type	L #	Hits	Search Text	DBs	Time Stamp
11	BRS	L11	37	10 and channel adj1 region	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2002/03/28 21:54
12	BRS	L12	13	11 and oxidation	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2002/03/28 21:59
13	BRS	L13	31	11 and oxid\$4	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2002/03/28 22:15
14	BRS	L14	5066	(transistor) near15 (dielectric adj1 layer or silicon adj1 dioxide)	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2002/03/28 22:46
15	BRS	L15	14	14	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2002/03/28 22:46

	Type	L #	Hits	Search Text	DBs	Time Stamp
17	ERS	L16	100	15 and channel	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2002/03/28 23:16
18	ERS	L17	69	16 and (source and drain)	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2002/03/28 23:17
19	ERS	L18	41	17 and gate nearl oxide\$1	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2002/03/28 23:16
19	ERS	L19	389	18 and transistor	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2002/03/28 23:18
20	ERS	L20	344	19 and thickness	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2002/03/28 23:18

	Type	L #	Hits	Search Text	DBs	Time Stamp
21	BRS	121	288	20 and channel	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2002/03/28 23:18
22	BRS	122	258	21 and (source and drain)	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2002/03/28 23:18
23	BRS	123	129	22 and oxidation	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2002/03/28 23:19
24	BRS	124	104	23 and second adj1	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2002/03/28 23:20
25	BRS	125	13	transistor	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2002/03/28 23:20

	U	1	Document ID	Title	Current OR
	<input type="checkbox"/>	<input type="checkbox"/>	US 20020004276 A1	Structure and method for dual gate oxide thicknesses	438/275
	<input type="checkbox"/>	<input type="checkbox"/>	US 20020004276 A1	Structure and method for dual gate oxide thicknesses	438/275
	<input type="checkbox"/>	<input type="checkbox"/>	US 20020004276 A1	Method of manufacturing semiconductor device in which hot carrier resistance can be improved and silicide layer can be formed with high reliability	438/275
	<input type="checkbox"/>	<input type="checkbox"/>	US 20020004276 A1	Structure and method for dual gate oxide thicknesses	438/275
	<input type="checkbox"/>	<input type="checkbox"/>	US 6232631 B1	Floating gate memory cell structure with programming mechanism outside the read path	257/315
	<input type="checkbox"/>	<input type="checkbox"/>	US 6048760 A	Method of forming a self-aligned refractory metal silicide contact using doped field oxide regions	438/225
7	<input type="checkbox"/>	<input type="checkbox"/>	US 5949706 A	Static random access memory cell having a thin film transistor (TFT) pass gate connection to a bit line	365/136
	<input type="checkbox"/>	<input type="checkbox"/>	US 5949706 A	Memory cell having a plural transistor transmission gate and method of formation	365/136.23
9	<input type="checkbox"/>	<input type="checkbox"/>	US 5777347 A	Vertical CMOS digital multi-valued restoring logic device	257/24
11	<input type="checkbox"/>	<input type="checkbox"/>	US 5257095 A	Common geometry high voltage tolerant long channel and high speed short channel field effect transistors	257/315
11	<input type="checkbox"/>	<input type="checkbox"/>	US 5045449 A	Method of making a high-speed 2-transistor cell for programmable/EEPROM devices with separate read and write transistors	438/258
11	<input type="checkbox"/>	<input type="checkbox"/>	US 4931411 A	Integrated circuit process with TiN-gate transistor	438/261

	U	1	Document ID	Title	Current OR
	<input type="checkbox"/>	<input type="checkbox"/>	US 4814854 A	Integrated circuit device and process with tin-gate transistor	2577352